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(71) Applicant *(for all designated States except US)*: **QUALCOMM, INCORPORATED** [US/US]; 5775 Morehouse Drive, San Diego, California 92121-1714 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **SMEE, John E.** [CA/US]; 5340 Toscana Way, Apt. F-406, San Diego, California 92122 (US). **ZHANG, Haitao** [CN/US]; 11018 Corte Mar De Delfinas, San Diego, California 92130 (US).

(74) Agents: **WADSWORTH, Philip R.** et al.; 5775 Morehouse Drive, San Diego, California 92121-1714 (US).

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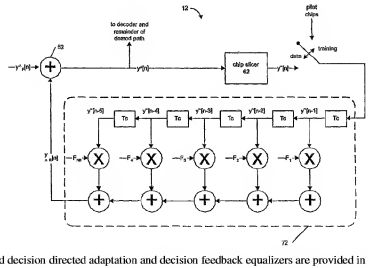
[Continued on next page]

(54) **Title:** IMPROVED SLICER INPUT AND FEEDBACK FILTER CONTENTS FOR BLOCK CODED DIGITAL COMMUNICATIONS



(57) **Abstract:** Improved decision directed adaptation and decision feedback equalizers are provided in a block coded digital communication system. The performance of a receiver is significantly improved by allowing the decision feedback equalizer to perform time-tracking and residual frequency offset compensation during the data portion of a frame. This is accomplished by capitalizing on the inherent correlation among the chips of a code word in a block coded digital communication system to identify certain instances where more reliable symbol estimates can be derived from a sliced chip without introduction the delay inherent in decoding. As the more reliable symbol estimates are fed back into the chip slicer, the total efficiency of the decision feedback equalizer is improved and the more reliable symbol estimates can be used to replace older content in the feedback filter to further improve the accuracy of the modified slicer input and further decrease the effects of error propagation by the decision feedback equalizer.

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IMPROVED SLICER INPUT AND FEEDBACK FILTER CONTENTS FOR BLOCK CODED DIGITAL COMMUNICATIONS

BACKGROUND

1. Field of the Invention

[01] The present invention relates generally to the field of wireless communications and more particularly relates to block coded digital communication systems.

2. Related Art

[02] Conventional block coded digital communication systems typically split a frame into known training symbols and known data symbols. Although the symbols are known, i.e., included in a predefined finite alphabet, the particular data symbols in any given frame are unknown to the receiver.

[03] During the training portion of a frame, it is well known to run tracking loops based on an error signal generated from the training data. For example, a time tracking loop or phase locked loop may be employed. Alternatively, or in combination, a least mean square ("LMS") equalizer updating procedure may also be used. These loops or procedures serve to provide critical information to the receiver of a wireless communication device.

[04] In these conventional block coded digital communication systems, it is often necessary to continue adapting the loops during the data portion of the frame, for example to compensate for a fading signal or timing error. A common method of such continuous adaptation is to employ decision-directed ("DD") adaptation. This scheme requires that the receiver estimate what symbols are received in the data stream. Typically, a slicer is employed to obtain tentative decisions for the transmitted data symbols and to determine the noise associated with the slicer decision. The final decisions for the transmitted data symbols are based on the decoder output.

[05] A problem associated with this scheme is the delay that is inherent in channel decoding. Because the symbols are encoded, the efficiency of the process is either reduced

by decoding the symbols or reduced by the higher error rate that is inherent with slicer decisions as opposed to decisions from the decoder output.

[06] Furthermore, implementing a decision feedback equalizer ("DFE") at the receiver to remove intersymbol interference ("ISI") exacerbates this problem because the input to the feedback filter ("FBF") comprises the higher error rate slicer decisions. Thus, when the sliced symbols that are put into the FBF are in error, which is more likely when they are encoded, then the DFE propagates the error and increases the likelihood of subsequent slicer errors and thereby diminishes performance. Fig. 1 is an example graph diagram illustrating conventional slicer errors when unmodified symbol estimates are used as slicer input.

[07] Therefore, what is needed is a method for improving slicer input and the corresponding feedback filter contents in block coded communications to overcome these significant problems found in the conventional systems as described above.

SUMMARY

[08] Methods for improved decision directed adaptation and decision feedback equalizers are presented. In a block coded digital communication system the performance of a receiver is significantly improved by allowing decision directed adaptation through a decision feedback equalizer to perform time-tracking and residual frequency offset compensation during the data portion of a frame. Additionally, DFE error propagation is decreased by modifying the contents of the feedback filter to include more reliable symbol estimates.

[09] As an encoded stream of symbols is received in a block coded digital communication system, a slicer is employed by a decision feedback equalizer to slice chips of a code word from the encoded stream and pass them to a feedback filter. Based on the inherent correlation among the chips of a code word, certain instances of more reliable symbol estimates are derived from the sliced chips.

[10] As the more reliable symbol estimates are fed back into the chip slicer, the total efficiency of the decision feedback equalizer is improved. Moreover, the more reliable symbol estimates are used to replace older content in the feedback filter to further improve

the accuracy of the modified slicer input and decrease the effects of DFE error propagation.

BRIEF DESCRIPTION OF THE DRAWINGS

[11] The details of the present invention, both as to its structure and operation, may be gleaned in part by study of the accompanying drawings, in which like reference numerals refer to like parts, and in which:

[12] **Figure 1** is an example graph diagram illustrating conventional slicer errors when unmodified symbol estimates are used as slicer input;

[13] **Figure 2** is a block diagram illustrating an example decision feedback equalizer according to an embodiment of the present invention;

[14] **Figure 3** is an example graph diagram illustrating a reduced amount of slicer errors based on modified symbol estimates according to an embodiment of the present invention;

[15] **Figure 4** is a block diagram illustrating an example chip slicer and feedback filter contents in a decision feedback equalizer according to an embodiment of the present invention;

[16] **Figure 5** is a table diagram illustrating improved feedback filter contents according to an embodiment of the present invention;

[17] **Figure 6A** is an example pseudo code listing for creating more accurate sliced chips for least mean square and feed back filter tracking according to an embodiment of the present invention;

[18] **Figure 6B** is an example pseudo code listing for using more accurate sliced chips for better least mean square updating of a decision feedback equalizer, feed forward filter, and feed back filter according to an embodiment of the present invention; and

[19] **Figure 6C** is an example pseudo code listing for using the more accurate sliced chips for improved feed back filter contents according to an embodiment of the present invention.

DETAILED DESCRIPTION

[20] Certain embodiments as disclosed herein provide for improved decision directed adaptation employed by a receiver in a block coded digital communication system. For example, one method as disclosed herein allows for the inherent correlation between the chips of a code word to be exploited to derive more reliable symbol estimates. These more reliable symbol estimates are then passed through a feedback filter to improve the accuracy of future input to the chip slicer. Additionally, the more reliable symbol estimates replace earlier symbol estimates in a feedback filter to further improve the total efficiency of the decision feedback equalizer.

[21] After reading this description it will become apparent to one skilled in the art how to implement the invention in various alternative embodiments and alternative applications. However, although various embodiments of the present invention will be described herein, it is understood that these embodiments are presented by way of example only, and not limitation. As such, this detailed description of various alternative embodiments should not be construed to limit the scope or breadth of the present invention as set forth in the appended claims.

[22] Fig. 2 is a block diagram illustrating an example decision feedback equalizer ("DFE") 10 according to an embodiment of the present invention. In the illustrated embodiment, the DFE 10 comprises an antenna 20, a preprocessor 30, a feed forward filter 40, a chip combiner 50, a chip slicer 60, and a feed back filter 70.

[23] The antenna 20 can be any of a variety of antennas configured for wireless communications in a block coded digital communication system, as will be understood by one having skill in the art. Similarly, the preprocessor 30 preferably carries out signal processing tasks and provides the feed forward filter 40 with baseband samples (i.e., digital input), as will also be understood by one having skill in the art. The feed forward filter 40 preferably processes the baseband samples and sends the digital data stream to the chip slicer 60, in combination with any signal added or subtracted by the chip combiner 50. In one embodiment, the feed back filter 70 can be a finite impulse response ("FIR") filter that processes the previous slicer 60 outputs to subtract out postcursor inter symbol interference ("ISI") from the current input to the slicer 60.

[24] In one embodiment, the length of the feedback filter 70 is not related to the length of the codewords. For example, the coefficients for the feed forward filter 40 and the feedback filter 70 can be selected based on the minimum mean square error ("MMSE") criterion using either adaptive techniques or based on computations involving a channel estimate.

[25] The chip slicer 60 is preferably configured to extract a portion of the data stream that corresponds to a single chip of a code word. Each sliced chip is preferably provided to the feed back filter 70, where the sliced chips are processed to determine any noise associated with the slicer decision. The feed back filter 70 advantageously feeds the noise component back into the chip slicer 60 by way of the chip combiner 50. In this fashion, the noise component can be subtracted from next incoming signal from the feed forward filter 40 before it is fed into the slicer 60.

[26] For example, in block coded digital communications, a stream of digital data is sent over the airwaves in analog form and received by the antenna 20. The analog waves are interpreted by the preprocessor 30 and converted to digital form. The digital signal comprises a frame that is divided into two portions, a training portion and a data portion. Within the data portion of the frame are a series of binary digits (i.e., ones and zeroes) that are encoded symbols which represent the data payload. These symbols can be broken down into a plurality of code words and each code word can be further broken down into a plurality of chips. For example, a complementary code keying ("CCK") code word, as specified for the IEEE 802.11b 5.5 Mb/s data rate, is eight (8) chips long.

[27] When an encoded symbol is sent to the chip slicer 60, the chip slicer 60 preferably identifies a subset of the symbol that represents a single chip. The correct identification of a chip is very important because if a chip is not correctly identified, then DFE error propagation will result, where the incorrectly sliced chips fed into the feedback filter 70 can result in an output from the feedback filter 70 that incorrectly accounts for interference and therefore causes further errors in slicer decisions made by the chip slicer 60.

[28] Thus, in the training portion of the frame, it is well known to provide information relating to the identification of chips. However, when signal strength fades, for example, the information provided in the training portion of the frame may become obsolete during processing of the data portion of the frame. To account for such variations in the signal

during the data portion of the frame, the chip slicer 60 sends the sliced chips to the feed back filter 70 in order to more accurately slice the next incoming chip.

[29] Advantageously, the construction of code words introduces a certain correlation between the various chips that comprise a code word. For example, a CCK code word is eight (8) chips long and includes the following structure:

[30] CCKchip(3) = CCKchip(1)

[31] CCKchip(4) = -CCKchip(2)

[32] CCKchip(5) = -CCKchip(7)

[33] CCKchip(6) = CCKchip(8)

[34] Knowledge of this structure allows the use of decision directed adaptation during the data portion of the frame in order to continuously calibrate the slicing of chips by the chip slicer 60. Thus, the symbol estimates created by the chip slicer 60 can be improved in fifty percent (50%) of the estimates according to:

[35] Improved_Estimate(3) = Estimate(3) + Estimate(1)

[36] Improved_Estimate(4) = Estimate(4) – Estimate(2)

[37] Improved_Estimate(7) = Estimate(7) – Estimate(5)

[38] Improved_Estimate(8) = Estimate(8) + Estimate(6)

[39] With the improved estimates from the slicer 60, an improved noise component can be fed back into the slicer 60 fifty percent (50%) of the time, resulting in significantly improved results and decreased DFE error propagation. Accordingly, Fig. 3 is an example graph diagram illustrating a reduced amount of slicer errors based on improved symbol estimates according to an embodiment of the present invention.

[40] Fig. 4 is a block diagram illustrating an example chip slicer 62 and feedback filter contents 72 in a decision feedback equalizer 12 according to an embodiment of the present invention. In the illustrated embodiment, the DFE 12 comprises a signal combiner 52, a chip slicer 62, and feed back filter 72. The feed back filter 72 comprises a series of tap contents that each contain decisions from the slicer 62. Each set of tap contents is shown

as "Tc" in Fig. 4. Advantageously, the DFE 12 can be switched so that the tap contents in the feed back filter 72 are updated only during the data portion of a frame.

[41] For certain block coded digital communication systems, for example, the IEEE 802.11b 5.5 Mb/s data rate system that uses CCK code words, the effects of DFE error propagation can be reduced by improving the reliability of slicer decisions that are stored in the tap contents of the feed back filter 72. In one embodiment, chips 3, 4, 7, and 8 of each CCK code word are known to contain more reliable information. Thus, these slicer decisions can be selectively fed back into the slicer 62 to improve the reliability of future slicer decisions.

[42] Additionally, once the slicer 62 has provided more reliable information, this information can be stored in the tap contents of the feed back filter 72 and the known correlation between the chips in the code word can be exploited to modify the older tap contents in the feed back filter 72 based on the more reliable information. For example, after slicing each of the chips 3, 4, 7, and 8 and placing them into the first tap contents of the feed back filter 72, the tap contents of the feed back filter 72 that is two chips old can be replaced with a more reliable value by modifying the third tap contents of the feed back filter 72. The tap contents are appropriately mixed and combined to create the new estimate to be fed to the chip slicer 62. Advantageously, after startup this ensures that the contents of feed back filter 72 taps 3 and higher will reflect the increased accuracy of the modified slicer input and thereby decrease DFE error propagation.

[43] For example, as k loops from 1 to 8 to represent the CCK chip index of the frame chip index n, the DFE may implement:

[44] If k = 3, $\bar{y}[n-3] = \bar{y}[n-1]$.

[45] If k = 4, $\bar{y}[n-3] = -\bar{y}[n-1]$.

[46] If k = 7, $\bar{y}[n-3] = -\bar{y}[n-1]$.

[47] If k = 8, $\bar{y}[n-3] = \bar{y}[n-1]$.

[48] Thus, as k loops from 1 to 8, the sample that is two chips old is modified pursuant to the correlation properties of the CCK code words as previously described in the CCKchip equations. After several chips have been processed, the majority of the tap

contents in feed back filter 72 will advantageously be based on the more accurate slicer input.

[49] Accordingly, Fig. 5 is a table diagram illustrating improved feedback filter contents according to an embodiment of the present invention. In the illustrated embodiment, the third and higher feed back filter tap contents reflect the improved accuracy of the chip estimates pursuant to the correlation between chips in the 8 chip CCK code words as previously described. Additionally, in the illustrated table, each row corresponds to a particular time index with time moving from top to bottom. Thus, the contents of feed back filter tap 9 are not modified until after the ninth row.

[50] Figs. 6A – 6C are example code sections in pseudo code that illustrate methods for improving slicer output, using the improved slicer output in various filters, and storing the improved slicer output in a feedback filter to decrease the effects of DFE error propagation. Specifically, Fig. 6A is an example pseudo code listing for creating more accurate sliced chips for least mean square and feed back filter tracking according to an embodiment of the present invention. Moreover, Fig. 6B is an example pseudo code listing for using more accurate sliced chips for better least mean square updating of a decision feedback equalizer, feed forward filter, and feed back filter according to an embodiment of the present invention. Furthermore, Fig. 6C is an example pseudo code listing for using the more accurate sliced chips for improved feed back filter contents according to an embodiment of the present invention.

[51] While the particular embodiment herein shown and described in detail is fully capable of attaining the above described objects of this invention, it is to be understood that the description and drawings presented herein represent a presently preferred embodiment of the invention and are therefore representative of the subject matter which is broadly contemplated by the present invention. It is further understood that the scope of the present invention fully encompasses other embodiments that may become obvious to those skilled in the art and that the scope of the present invention is accordingly limited by nothing other than the appended claims.

WHAT IS CLAIMED IS:

CLAIMS

1. A method for improved digital communications, comprising:

receiving a frame in a digital communications stream, the frame having a training portion and a data portion, wherein the data portion comprises an encoded symbol, the encoded symbol having a plurality of code words, wherein each code word has a plurality of chips;

slicing a chip from the encoded symbol;

removing interference from the chip;

deriving a more accurate symbol estimate for the sliced chip based on a correlation among the chips in the code word; and

providing the more accurate symbol estimate as input to the chip slicer.

2. The method of claim 1, wherein the receiving step further comprises receiving the encoded symbol during the data portion of a frame.

3. The method of claim 2, wherein the providing step comprises decision directed updating during the data portion of a frame.

4. The method of claim 1, wherein at least fifty percent of the symbol estimates provided to the chip slicer are more accurate.

5. The method of claim 1, further comprising:

providing the more accurate symbol estimate to the feedback filter; and

storing the more accurate symbol estimate in the feedback filter.

6. The method of claim 5, where in the removing step further comprises using the more accurate symbol estimate stored in the feedback filter for improved performance in removing interference from the chip.

7. The method of claim 5, wherein at least fifty percent of the symbol estimates stored in the feedback filter are more accurate.

8. The method of claim 1, wherein the method is repeated to create more reliable symbol estimates relative to older symbol estimates already derived, and wherein the more reliable symbol estimates are used in a feedback filter to improve the accuracy of the symbol estimates being fed into the chip slicer.

9. A system for improved digital communications, comprising:

a chip slicer for extracting a chip from a code word, the code word received as part of an encoded symbol in a digital communication stream;

a feed back filter configured to remove interference from sliced chips, the feedback filter having a plurality of content registers; and

a chip combiner configured to derive a more accurate symbol estimate for a sliced chip, wherein the chip combiner provides improved symbol estimates to the chip slicer.

10. The system of claim 9, wherein one or more content registers are updated with more accurate symbol estimates during decision directed updating.

11. The system of claim 10, wherein the majority of the plurality of content registers contain more accurate symbol estimates.

12. The system of claim 9, wherein the feed back filter is a finite impulse response ("FIR") filter, wherein the FIR subtracts out postcursor inter-symbol interference from the current slicer input.

13. The system of claim 9, wherein the chip combiner derives a more accurate symbol estimate based on a correlation among the chips in the code word.

14. A receiver for use in a block coded digital communications system, comprising:

a preprocessor for carrying out signal processing tasks and for providing a feed forward filter with baseband samples;

the feed forward filter for processing the baseband samples and for sending a digital data stream to a chip slicer in combination with any signal added or subtracted by a chip combiner; and

a feedback filter for processing previous chip slicer outputs to subtract out postcurser inter symbol interference from the current input to the chip slicer.

15. The receiver of claim 14, wherein coefficients for the feed forward filter and the feedback filter are selected based on minimum mean square error (MMSE) criterion using either adaptive techniques or based on computations involving a channel estimate.

16. The receiver of claim 14, wherein the chip slicer is configured to extract a portion of the data stream that corresponds to a single chip of a code word.

17. The receiver of claim 14, wherein the feedback filter feeds the noise component back into the chip slicer by way of a chip combiner so that the noise component can be subtracted from the next incoming signal from the feed forward filter before the next incoming signal is fed into the chip slicer.

18. A receiver for use in a block coded digital communications system, comprising:

means for receiving a frame in a digital communications stream, the frame having a training portion and a data portion, wherein the data portion comprises an encoded symbol, the encoded symbol having a plurality of code words, wherein each code word has a plurality of chips;

means for slicing a chip from the encoded symbol;

means for removing interference from the chip;

means for deriving a more accurate symbol estimate for the sliced chip based on a correlation among the chips in the code word; and

means for providing the more accurate symbol estimate as input to the chip slicer.

19. The receiver of claim 18, wherein the means for slicing a chip from the encoded symbol further comprises a chip slicer for extracting a chip from a code word, the code word received as part of an encoded symbol in a digital communication stream.

20. The receiver of Claim 19, wherein the means for removing interference from the chip further comprising a feed back filter configured to remove interference from sliced chips, the feed back filter having a plurality of content registers.

21. The receiver of claim 20, wherein the means for deriving a more accurate symbol estimate for the sliced chip based on a correlation among the chips in the code word further comprises a chip combiner configured to derive a more accurate symbol estimate

for a sliced chip, and wherein the chip combiner provides improved symbol estimates to the chip slicer.

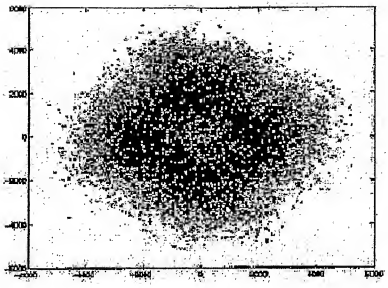

FIG. 1

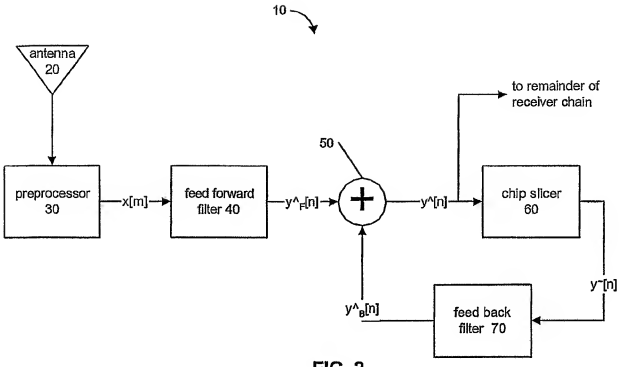
10
antenna 20
preprocessor 30
x[m]
feed forward filter 40
y^F[n]
50
y^[n]
to remainder of receiver chain
chip slicer 60
y~[n]
y^B[n]
feed back filter 70

FIG. 2

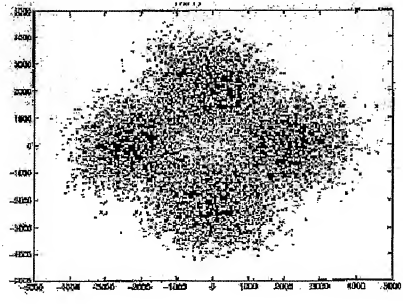

FIG. 3

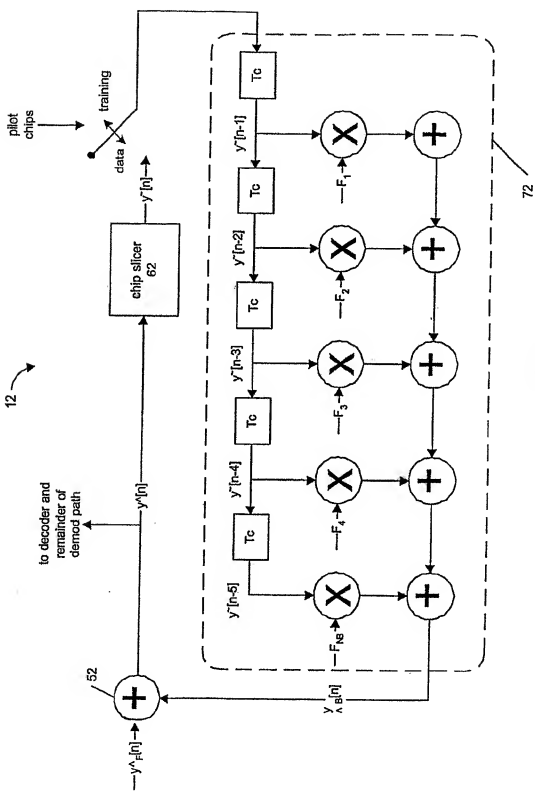
12
pilot chips
training
data
chip slicer 62
y^[n]
to decoder and remainder of demod path
y^[n]
52
y^_R[n]
y^_Bl[n]
Tc
y^[n-1]
y^[n-2]
y^[n-3]
y^[n-4]
y^[n-5]
F1
F2
F3
F4
FNB
72

FIG. 4

content of FBF tap 9	content of FBF tap 8	content of FBF tap 7	content of FBF tap 6	content of FBF tap 5	content of FBF tap 4	content of FBF tap 3	content of FBF tap 2	content of FBF tap 1	slicer input at time (n)	CCK chip index (k)	frame chip index (n)
									1	1	1
								1	2	2	2
							1	2	3with1	3	3
						1from3	2	3with1	4with2	4	4
					1from3	2from4	3with1	4with2	5	5	5
				1from3	2from4	3with1	4with2	5	6	6	6
			1from3	2from4	3with1	4with2	5	6	7with5	7	7
		1from3	2from4	3with1	4with2	5from7	6	7with5	8with6	8	8
	1from3	2from4	3with1	4with2	5from7	6from8	7with5	8with6	9	1	9
1from3	2from4	3with1	4with2	5from7	6from8	7with5	8with6	9	10	2	10
2from4	3with1	4with2	5from7	6from8	7with5	8with6	9	10	11with9	3	11
3with1	4with2	5from7	6from8	7with6	8with6	9from11	10	11with9	12with10	4	12
4with2	5from7	6from8	7with5	8with6	9from11	10from12	11with9	12with10	13	5	13
5from7	6from8	7with5	8with6	9from11	10from12	11with9	12with10	13	14	6	14
6from8	7with5	8with6	9from11	10from12	11with9	12with10	13	14	15with13	7	15
7with5	8with6	9from11	10from12	11with9	12with10	13from15	14	15with13	16with14	8	16
8with6	9from11	10from12	11with9	12with10	13from15	14from16	15with13	16with14	17	1	17
9from11	10from12	11with9	12with10	13from15	14from16	15with13	16with14	17	18	2	18
10from12	11with9	12with10	13from15	14from16	15with13	16with14	17	18	19with17	3	19
11with9	12with10	13from15	14from16	15with13	16with14	17from19	18	19with17	20with18	4	20
12with10	13from15	14from16	15with13	16with14	17from19	18from20	19with17	20with18	21	5	21

FIG. 5

```
%%add new section to do 5.5M slicing based on CCK codeword knowledge (1=3, 2=-4, 5=-7, 6=8)
if MPDU_RATE= =5.5 & kk= =3
        slicer_output=hard_decision(real(chipCx1_estimate_vec(kk)+chipCx1_estimate_vec(kk-2)), ...
        imag(chipCx1_estimate_vec(kk)+chipCx1_estimate_vec(kk-2)));
elseif MPDU_RATE= = 5.5 & kk= =4
        slicer_output=hard_decision(real(chipCx1_estimate_vec(kk)-chipCx1_estimate_vec(kk-2)), ...
        imag(chipCx1_estimate_vec(kk)-chipCx1_estimate_vec(kk-2)));
elseif MPDU_RATE= = 5.5 & kk= =7
        slicer_output=hard_decision(real(chipCx1_estimate_vec(kk)-chipCx1_estimate_vec(kk-2)), ...
        imag(chipCx1_estimate_vec(kk)-chipCx1_estimate_vec(kk-2)));
elseif MPDU_RATE= = 5.5 & kk= =8
        slicer_output=hard_decision(real(chipCx1_estimate_vec(kk)+chipCx1_estimate_vec(kk-2)), ...
        imag(chipCx1_estimate_vec(kk)+chipCx1_estimate_vec(kk-2)));
end
```

FIG. 6A

```
If (kk= =3 | kk = = 4 | kk= =7 | kk = = 8) % use slicer output for improved DD-LMS on FFF
        FFF = FFF +LMS_stepsize*(FFF_content_I_Cx2+j*FFF_contentQ_Cx2)
*conj(train_scale*slicer_output-chipCx1_estimate_vec(kk));

If (kk= =3 | kk = = 4 | kk= =7 | kk = = 8) % use slicer output for improved DD-LMS on FBF
        FBF = FBF +LMS_stepsize*(FBF_content1_Cx1+j*FBF_contentQ_Cx1)
*conj(train_scale*slicer_output-chipCx1_estimate_vec(kk))
```

FIG. 6B

```
FBF_contentI_Cx1 = [FBF_input_scale*real(slicer_output); FBF_contentI_Cx1 (1:end-1)];
FBF_contentQ_Cx1 = [FBF_input_scale*imag(slicer_output);FBF_contentQ_Cx1(1:end-1)];

%% Add Section to modify FBF contents based on more accurate sliced value. (i.e. on chips 3, 4, 7, 8
%% we have better information on the FBF contents that are 2 chips old, so we replace FBF(3) with the
%% appropriately signed version of FBF(1))

if kk = = 3
        FBF_content1_Cx1(3)=FBF_contentI_Cx1(1);
        FBF_contentQ_Cx1(3)=FBF_contentQ_Cx1(1);
elseif kk = = 4
        FBF_content1_Cx1(3)=-FBF_contentI_Cx1(1);
        FBF_contentQ_Cx1(3)=-FBF_contentQ_Cx1(1);
elseif kk = = 7
        FBF_content1_Cx1(3)=-FBF_contentI_Cx1(1);
        FBF_contentQ_Cx1(3)=-FBF_contentQ_Cx1(1);
elseif kk = = 8
        FBF_content1_Cx1(3)=FBF_contentI_Cx1(1);
        FBF_contentQ_Cx1(3)=FBF_contentQ_Cx1(1);
end
```

FIG. 6C

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(71) Applicant *(for all designated States except US)*: QUALCOMM, INCORPORATED [US/US]; 5775 Morehouse Drive, San Diego, California 92121-1714 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: SMEE, John E. [CA/US]; 5340 Toscana Way, Apt. F-406, San Diego, California 92122 (US). ZHANG, Haitao [CN/US]; 11018 Corte Mar De Definas, San Diego, California 92130 (US).

(74) Agents: WADSWORTH, Philip R. et al.; 5775 Morehouse Drive, San Diego, California 92121-1714 (US).

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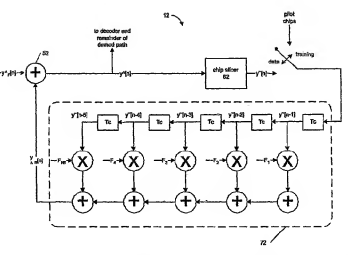
[Continued on next page]

(54) Title: METHOD AND APPARATUS FOR IMPROVING THE EQUALISATION OF BLOCK CODED SIGNALS



(57) Abstract: Improved decision directed adaptation and decision feedback equalizers are provided in a block coded digital communication system. The performance of a receiver is significantly improved by allowing the decision feedback equalizer to perform time-tracking and residual frequency offset compensation during the data portion of a frame. This is accomplished by capitalizing on the inherent correlation among the chips of a code word in a block coded digital communication system to identify certain instances where more reliable symbol estimates can be derived from a sliced chip without introduction the delay inherent in decoding. As the more reliable symbol estimates are fed back into the chip slicer, the total efficiency of the decision feedback equalizer is improved and the more reliable symbol estimates can be used to replace older content in the feedback filter to further improve the accuracy of the modified slicer input and further decrease the effects of error propagation by the decision feedback equalizer.

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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	WO 00/72540 A (HOME WIRELESS NETWORKS INC) 30 November 2000 (2000-11-30)	1,4-9, 12-21 2,3,10, 11
Y	US 6 426 972 B1 (HULYALKAR SAMIR N ET AL) 30 July 2002 (2002-07-30) column 1, line 62 - line 67 column 5, line 29 - line 45 column 7, line 13 - line 20	2,3,10, 11
P,X	US 2004/101068 A1 (LEE CHUN-HSIEN ET AL) 27 May 2004 (2004-05-27) paragraph '0009!	1-21

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information on patent family members

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Patent document cited in search report		Publication date	Patent family member(s)		Publication date
WO 0072540	A	30-11-2000	AU 5024300 A		12-12-2000
			EP 1188283 A1		20-03-2002
			WO 0072540 A1		30-11-2000
US 6426972	B1	30-07-2002	NONE		
US 2004101068	A1	27-05-2004	NONE		